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APPLICATION FOR PATENT

APPARATUS AND METHOD FOR REORDERING SEQUENCE INDICATED INFORMATION UNITS INTO PROPER SEQUENCE

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FIELD OF THE INVENTION

The present invention generally relates to techniques for sorting sequential information into proper sequence and in particular, to an apparatus and method for reordering sequence indicated information units into proper sequence.

BACKGROUND OF THE INVENTION

Certain applications require received information units to be sorted into proper sequence. For example, where the information units had been transmitted in proper sequence, but received out of sequence, then it is commonly necessary to resort or reorder the information units back into their proper sequence. Although there are numerous sorting algorithms commonly available for sorting sequence indicated information units in the software domain, in certain applications, an efficient and simple to implement hardware solution is desirable to meet system performance requirements.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an easily implemented apparatus for

reordering sequence indicated information units into proper sequence.

Another object is to provide a high performance apparatus for reordering sequence indicated information units into proper sequence.

Another object is to provide a reliable apparatus for reordering sequence indicated information units into proper sequence.

Another object is to provide a method for reordering sequence indicated information units into proper sequence that results in high performance operation when implemented in hardware.

These and additional objects are accomplished by the various aspects of the present invention, wherein briefly stated, one aspect of the invention is an apparatus for reordering sequence indicated information units into proper sequence. The apparatus includes a double-back shifter receiving sequence indicated information units, and at least one circuit coupled to the double-back shifter to repetitively compare, reorder and shift the sequence indicated information units so as to be in proper sequence when shifted out of the double-back shifter. In a preferred embodiment, the double-back shifter includes two rows of storage units configured such that an output of one row is shifted into the other row as input and the two rows shift their stored contents in opposite directions.

In another aspect, a method for reordering sequence indicated information units into proper sequence, comprises: repetitively comparing, reordering and shifting sequence indicated information units in a double-back shifter so as to be in proper sequence when shifted out of the double-back shifter. The sequence indicated information

units being compared and the associated sequence indicated information units that are being reordered in light of such comparison depend upon the mode of operation of the method. The mode of operation is preferably determined by: whether a double shift or single shift method is employed; the number of columns shifted during each shift; whether the comparing, reordering and shifting are performed in a single operation; and whether the incoming sequence indicated information units are a limited or continuous stream of information units.

Additional objects, features and advantages of the various aspects of the present invention will become apparent from the following description of its preferred embodiment, which description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates, as an example, a block diagram of portions of a SONET network element.

FIG. 2 illustrates, as an example, a block diagram of portions of a SONET network element including an apparatus utilizing aspects of the present invention.

FIG. 3 illustrates, as an example, a block diagram of a cell reorder apparatus for reordering sequence indicated information units into proper sequence, utilizing aspects of the present invention.

FIG. 4 illustrates, as an example, sequence indicators included with information units stored in a 4-cell outgoing buffer.

FIG. 5 illustrates, as an example, sequence indicators included with information units stored in a 4-cell incoming buffer.

FIGS. 6A~6N illustrate a simplified example of a single column, double shift mode of operation on a limited stream of incoming information units, utilizing aspects of the present invention.

FIG. 7 illustrates, as an example, sequence indicators included with information units being shifted out of the cell reorder apparatus utilizing aspects of the present invention.

FIGS. 8A~8B illustrate, as an example, a single column, double shift mode of operation utilizing aspects of the present invention.

FIGS. 9A~9B illustrate, as an example, a double column, double shift mode of operation utilizing aspects of the present invention.

FIGS. 10A~10D illustrate a simplified example of the double column, double shift mode of operation on a limited stream of incoming information units, utilizing aspects of the present invention.

FIG. 11 illustrates, as an example, a single column, single shift mode of operation utilizing aspects of the present invention.

FIGS. 12A~12H illustrate a simplified example of the single column, single shift mode of operation on a limited stream of incoming information units, utilizing aspects of the present invention.

FIG. 13 illustrates, as another example, a block diagram of portions of a SONET network element including an apparatus utilizing aspects of the present invention.

FIG. 14 illustrates, as an example, a block diagram including further detail on the relationship of the incoming buffers, the staging shifter and the reorder unit, utilizing aspects of the present invention.

FIG. 15 illustrates, as an example, a flow diagram of a method for reordering sequence indicated information units into proper sequence employing a single column, double shift mode of operation on a limited stream of incoming information units, utilizing aspects of the present invention.

FIG. 16 illustrates, as an example, a flow diagram of a method for reordering sequence indicated information units into proper sequence employing a single column, double shift mode of operation on a continuous stream of incoming information units, utilizing aspects of the present invention.

FIG. 17 illustrates, as an example, a flow diagram of a method for reordering sequence indicated information units into proper sequence employing a single column, single shift mode of operation on a continuous stream of incoming information units, utilizing aspects of the present invention.

FIG. 18 illustrates, as an example, a flow diagram of a method for reordering sequence indicated information units into proper sequence employing a combined single column, single shift mode of operation on a continuous stream of incoming information units, utilizing aspects of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

One important example of an application employing the present invention is in a synchronous optical network ("SONET") or synchronous digital hierarchy ("SDH") network element such as the SONET or SDH network element partially depicted in **FIG. 1.** In this application, information units in the form of cells or payloads are stored in an outgoing buffer **102** of a source **101** for transmission to an incoming buffer **104** of a destination **103** through a distributed switch fabric including representative switch slices **105~109.**

Although it is advantageous for the switch slices to operate asynchronously, such asynchronous operation increases the likelihood that the cells will arrive out of sequence at the incoming buffer **104.** For example, different delays in transit from the outgoing buffer **102** to the incoming buffer **104** may result from clock differences between switch slices in the distributed switch fabric, as different cells take different routes through the distributed switch fabric. For example, one cell might be transmitted through switch slice **105** having a certain clock frequency while another cell might be transmitted through switch slice **106** having a slightly higher or lower clock frequency than that of switch slice **105.** If the switch fabric is included in a multi-shelf system, then additional differences in transit delays may also result from different switch slices being located on different shelves in the system.

To avoid such problems with asynchronous systems, a synchronous or common clock system may be employed in the SONET NE. Such synchronous systems, however, are generally much more complicated to implement and therefore, much more expensive to manufacture than a corresponding asynchronous

system. Synchronous systems are particularly more difficult to implement in a multi-shelf system. They are also prone to be less reliable than corresponding asynchronous systems, because of their added complexity.

Accordingly, the present invention is particularly useful in facilitating a multi-shelf distributed switch fabric including asynchronously operating switch slices in a SONET or SDH network element. It is therefore noted that the following description and claimed aspects of the present invention are applicable to synchronous optical networks (SONET), synchronous digital hierarchy (SDH) networks, as well as other applications. As for SONET and SDH networks, the term SONET, as used herein, shall be understood to include both SONET and SDH to simplify the following description and claims.

FIG. 2 illustrates, as an example, a block diagram of portions of a SONET network element including an apparatus identified as cell reorder unit **200**. The cell reorder unit **200** reorders the received information units stored in incoming buffer **104** into proper sequence according to sequence information included in the received information units. The reordered information units may then be sent directly to other circuitry in the destination **103** for continued processing.

FIG. 3 illustrates, as an example, a block diagram of one version of a cell reorder unit or apparatus **200** for reordering sequence indicated information units into proper sequence, employing a single column, double shift mode of operation. A first plurality of serially coupled storage units (including representative storage units **201~206**) function as a first shifter responsive to an upper row enable signal SEN1, and a second plurality of serially

coupled storage units (including representative storage units **207~212**) function as a second shifter responsive to a lower row enable signal SEN2. Each of the storage units (e.g., **201~212**) is capable of storing an information unit such as, in this case, a sequence indicator, a source indicator, a payload location pointer, and a valid entry indicator for a SONET payload or cell.

A last storage unit **206** of the first plurality of serially coupled storage units is coupled to a first storage unit **207** of the second plurality of serially coupled storage units so that an information unit shifted out of the storage unit **206** is shifted into the storage unit **207**. Coupled together in this fashion, the first and second pluralities of serially coupled storage units function and are referred to herein as a double-back shifter. For convenience in the following description and claims, the first plurality of serially coupled storage units (including representative storage units **201~206**) is referred to herein as a first shifter or a top or upper row of the double-back shifter, and the second plurality of serially coupled storage units (including representative storage units **207~212**) is referred to as a second shifter or a bottom or lower row of the double-back shifter. A key feature of the double-back shifter is that the top row shifts in one direction (e.g., from right to left in this example), and the bottom row shifts in an opposite direction (e.g., from left to right in this example). The operation mode in this example is referred to as being a double shift, because the top and bottom rows of the double-back shifter are shifted independently and at different times.

Compare and reorder logic, comprising, in this example, a plurality of compare and reorder elements or circuits (including representative elements **213~218**), is

also included in this version of the cell reorder unit **200**. Each compare and reorder element is coupled to a corresponding pair of storage units from the first and second pluralities of serially coupled storage units. The corresponding pairs are generated by pairing storage units in a shifting order (e.g., **201~206**) of the first plurality of serially coupled storage units with storage units in a reverse shifting order (e.g., **212~207**) of the second plurality of serially coupled storage units. For example, in the double-back shifter configuration depicted in **FIG. 3**, the corresponding pairs are formed by corresponding positions of the first and second rows (i.e., storage cells in a same column of the two rows).

Each of the plurality of compare and reorder elements functions to read and compare sequence information included in information units stored in its corresponding pair, and reorder the information units into their proper sequence if the comparison indicates that the information units are out of sequence, are valid information units, and are from the same source.

The plurality of compare and reorder elements perform their function following each shift of the top and bottom row of the double-back shifter. After stored information units are alternately shifted in the top and bottom rows, and processed following each shift by the plurality of compare and reorder elements, the information units are eventually found reordered into proper sequence by the time they are completely shifted out of the second row of the double-back shifter.

To illustrate the operation of the reorder cell unit **200** in a single column, double shift mode of operation for a limited stream of incoming information units, **FIGS.**

4~7 are now described. **FIG. 4** illustrates, for this simplified example, sequence indicators that are included in information units stored in a 4-cell outgoing buffer **102** of the source **101**. As previously described, these information units are then transmitted to an incoming buffer **104** of the destination **103** through the distributed switch fabric including representative switch slices **105~109**. **FIG. 5** illustrates sequence indicators included in the received information units as stored in a 4-cell incoming buffer **104** of the destination **103**. Note that the information unit stored in storage unit **504** has arrived out of sequence in this example, having arrived before information units stored in storage units **502** and **503** rather than after those units as it was supposed to.

FIGS. 6A~6N illustrate, as examples, the sequence indicators of the information units and their locations in various stages of their processing by the **FIG. 3** version of the cell reorder unit **200**. In **FIG. 6A**, the information units stored in the incoming buffer **104** are shown shifted into the top row of the double-back shifter from the incoming buffer **104**. The top row comprising serially coupled storage cells **601~604**, in this example, also has a length of 4-cells for convenience in this description, although generally it would be longer to account for skew and other considerations in the system. In **FIG. 6B**, contents of the first row are shown as each being shifted one storage unit to the left, except the contents of the last storage unit **604**, which is shown being shifted into the first storage unit **605** of the second row. In **FIG. 6C**, contents of the first and second rows are shown after the compare and reorder element **609** has performed its function. In particular, the compare and reorder element **609** has read

the sequence information in its corresponding pair of storage units, **604** and **605**, and determined that they are out of sequence since the sequence indicator 1 in this case should be before the sequence indicator 3. As a result, the compare and reorder element **609** has reordered or swapped the contents of storage units **604** and **605** in this case so that they are placed in the proper sequence. Compare and reorder elements **610**, **611** and **612** have not performed any reordering since storage units **606**, **607**, **601** and **608**, in this example, are presumed to contain invalid information units, and the compare and reorder elements **609~612** only process valid information units from the same source.

In **FIG. 6D**, contents of the second row are shown being shifted one storage unit to the right. In **FIG. 6E**, contents of the first and second rows are shown after the compare and reorder element **610** has performed its function. In particular, the compare and reorder element **610** has read the sequence information in its corresponding pair of storage units, **603** and **606**, and determined that they are in sequence since the sequence indicator 1 in this case is and should be before the sequence indicator 2. As a result, the compare and reorder element **610** has left the contents of storage units **603** and **606** alone since they are already in the proper sequence. Meanwhile, compare and reorder elements **609**, **611** and **612** have not performed any reordering since storage units **605**, **607**, **601** and **608**, in this example, are presumed to contain invalid information units.

In **FIG. 6F**, contents of the first row are shown as each being shifted one storage unit to the left again, except the contents of the last storage unit **604**, which is shown being shifted into the first storage unit **605** of the second row. In **FIG. 6G**, contents of the first and second

rows are shown after the compare and reorder elements **609** and **610** have performed their functions. In particular, the compare and reorder element **609** has read the sequence information in its corresponding pair of storage units, **604** and **605**, and determined that they are out of sequence since the sequence indicator 2 in this case should be before the sequence indicator 3. As a result, the compare and reorder element **609** has reordered or swapped the contents of storage units **604** and **605** in this case to be in the proper sequence, so that the information unit having the sequence indicator 3 is now in storage unit **604** and the information unit having the sequence indicator 2 is now in storage unit **605**. Meanwhile, the compare and reorder element **610** has read the sequence information in its corresponding pair of storage units, **603** and **606**, and determined that they are in sequence since the sequence indicator 1 in this case is and should be before the sequence indicator 4. As a result, the compare and reorder element **610** has left the contents of storage units **603** and **610** alone since they are already in the proper sequence. Meanwhile, compare and reorder elements **611** and **612** have not performed any reordering since storage units **601, 602, 607** and **608**, in this example, are presumed to contain invalid information units.

In **FIG. 6H**, contents of the second row are shown being shifted one storage unit to the right. In **FIG. 6I**, contents of the first and second rows are shown after the compare and reorder element **610** has performed its function. In particular, the compare and reorder element **610** has read the sequence information in its corresponding pair of storage units, **603** and **606**, and determined that they are in sequence since the sequence indicator 2 in this case is and should be before the sequence indicator 4. As a result, the

compare and reorder element **610** has left the contents of storage units **603** and **606** alone since they are already in the proper sequence. Meanwhile, compare and reorder elements **609, 611** and **612** have not performed any reordering since storage units **605, 602, 601** and **608,** in this example, are presumed to contain invalid information units.

In **FIG. 6J,** contents of the first row are shown as each being shifted one storage unit to the left, except the contents of the last storage unit **604,** which is shown being shifted into the first storage unit **605** of the second row. In **FIG. 6K,** contents of the first and second rows are shown after the compare and reorder element **609** has performed its function. In particular, the compare and reorder element **609** has read the sequence information in its corresponding pair of storage units, **604** and **605,** and determined that they are in sequence since the sequence indicator 3 in this case is and should be before the sequence indicator 4. As a result, the compare and reorder element **609** has left the contents of storage units **604** and **605** alone in this case since they are already in the proper sequence. Meanwhile, compare and reorder elements **610, 611** and **612** have not performed any reordering since storage units **603, 602, 601** and **608,** in this example, are presumed to contain invalid information units.

In **FIG. 6L,** contents of the second row are shown being shifted one storage unit to the right again. In **FIG. 6M,** contents of the first and second rows are shown unchanged this time after the compare and reorder elements **609~612** have performed their functions. In this case, no reordering has been performed by any of the compare and reorder elements, because storage units **605, 603, 602** and **601,** in this example, are presumed to contain invalid

information units. In **FIG. 6N**, contents of the first and second rows are shown after the information unit stored in the last storage unit **604** in the first row has been shifted into the first storage unit **605** of the second row. The information units contained in storage units **605~608** of the second row are now in proper sequence. **FIG. 7** then illustrates the sequence indicators being in proper sequence for the information units that have been shifted out of the second row of the double-back shifter.

Although the example described above in reference to **FIGS. 4~7** referred to "swapping contents" of storage units, it is to be appreciated that reordering of information units may be performed by various well-known techniques including swapping contents, swapping pointers, and effectively coupling and decoupling of storage units from one row to another by using, for example, multiplexer circuits controlled by the compare and reorder logic. Also, although the example described above performs a shift before a compare and reorder, these two operations may be reversed and/or performed in a same operation. Further, although the example described a double shift mode of operation wherein the top row was shifted prior to shifting the bottom row, the order of shifting may be reversed.

FIGS. 8A~8B illustrate, for example, a single column, double shift mode of operation, wherein the compare and reorder step and the shift step have been combined into a single macro step. In **FIG. 8A**, a compare and reorder element, circuit or logic **811** compares sequence indicators stored in corresponding storage units **801** and **802**, then stores the information unit with the higher (later sequenced) one in storage unit **801** and shifts the information unit with the lower (earlier sequenced) one into

associated storage unit **804**, which is one column to the right of storage unit **802** on the bottom row. (Note, however, that if the storage unit **802** is the last storage unit in the bottom row of the double-back shifter, then the information unit with the lower sequence indicator is instead shifted out of the double-back shifter.) Meanwhile, another compare and reorder element to the left of the compare and reorder element **811** (or an extension of the compare and reorder element **811**) is performing a similar function to update the contents of storage unit **802**.

In **FIG. 8B**, the compare and reorder element **811** compares sequence indicators stored in corresponding storage units **801** and **802**, then stores the information unit with the lower one in storage unit **802** and shifts the information unit with the higher one into associated storage unit **803**, which is one column to the left of storage unit **801** on the top row. (Note, however, that if the storage unit **801** is the last storage unit in the top row of the double-back shifter, then the information unit with the higher sequence indicator is instead shifted into the storage unit **802**, which, in that case would be the first storage unit in the bottom row.) Meanwhile, another compare and reorder element to the right of the compare and reorder element **811** (or an extension of the compare and reorder element **811**) is performing a similar function to update the contents of storage unit **801**.

Although the prior examples described single column shifts, multiple column shifts may also be performed in the present invention. **FIGS. 9A~9B** illustrate, as an example, a double column, double shift mode of operation, wherein the compare and reorder step and the shift step have been combined into a single macro step. In **FIG. 9A**, a

compare and reorder element, circuit or logic **911** compares sequence indicators stored in corresponding storage units **901**, **902**, **903** and **904**, then stores a highest one in storage unit **901**, stores a second highest one in storage unit **903**, shifts a lowest one into associated storage unit **908**, and shifts a second lowest one into associated storage unit **906**. Associated storage units **906** and **908** are respectively two and one columns to the right of storage unit **904** on the bottom row, and therefore, by updating their contents at the same time, a double column shift is performed. (Note, however, that if the storage units **902** and **904** are the last storage units in the bottom row of the double-back shifter, then the information units with the lower and second lowest sequence indicators are instead shifted out of the double-back shifter.) Meanwhile, another compare and reorder element to the left of the compare and reorder element **911** (or an extension of the compare and reorder element **911**) is performing a similar function to update the contents of storage units **902** and **904**.

In **FIG. 9B**, the compare and reorder element **911** compares sequence indicators stored in corresponding storage units **901**, **902**, **903** and **904**, then stores a lowest one in storage unit **904** and a second lowest one in storage unit **902**, and shifts a highest one into associated storage unit **905** and a second highest one into associated storage unit **907**, which are respectively two and one columns to the left of storage unit **903** on the top row. (Note, however, that if the storage units **901** and **903** are the last storage units in the top row of the double-back shifter, then the information unit with the highest sequence indicator is instead shifted into the storage unit **902** and the information unit with the second highest sequence indicator is shifted into the

storage unit **904**, which would be the second and first storage units in the bottom row.) Meanwhile, another compare and reorder element to the right of the compare and reorder element **911** (or an extension of compare and reorder element **911**) is performing a similar function to update the contents of storage units **901** and **903**.

FIGS. 10A~10D illustrate, as a simplified example, the operation of a second version of the reorder cell unit **200**, employing a double column, double shift mode of operation for a limited stream of incoming information units. In **FIG. 10A**, the first row of a double-back shifter including storage units **1001~1008** is shown storing sequence indicators that are out of sequence. In **FIG. 10B**, after execution of a double column shift, the contents of top row storage units **1004** and **1003** have been respectively shifted into bottom row storage units **1006** and **1005**. No comparison and reorder operations had been performed in this case, because storage units **1005~1008** are assumed to contain invalid entries. In **FIG. 10C**, compare and reorder logic **1012** (comprising at least one circuit) compares sequence indicators stored in corresponding storage units **1003~1006**, and reorders the contents of those storage units such that the information unit with the highest sequence indicator is stored in storage unit **1003** (in this case, the information unit having the sequence indicator of 4), the information unit with the second highest sequence indicator is stored in storage unit **1004** (in this case, the information unit having the sequence indicator of 3), the information unit with the lowest sequence indicator is shifted into storage unit **1008** (in this case, the information unit having the sequence indicator of 1), and the information unit with the second lowest sequence indicator is shifted into storage unit **1007**

(in this case, the information unit having the sequence indicator of 2). In **FIG. 10D**, after execution of a double column shift, the contents of top row storage units **1004** and **1003** have been respectively shifted into bottom row storage units **1006** and **1005**. No comparison and reorder operations had been performed in this case, because storage units **1001~1002** corresponding to storage units **1008~1007** and storage units **1005~1006** corresponding to storage units **1004~1003** are assumed to contain invalid entries. As is evident by inspection of the bottom row of the double-back shifter, contents are now in proper sequence in the bottom row.

By extending the at least one circuit described above in reference to **FIGS. 8A~8B** and **9A~9B**, compare and reorder operations for higher number column shifts are readily determinable. Although the implementation for such higher number column shift versions get increasingly more complex, the added complexity may be justified in situations where execution speed and/or bandwidth are critical.

Although the prior examples described double shift operations with alternating top and bottom or bottom and top row shifts, single shift operations may also be performed in the present invention. In this case, the operation is referred to as being a single shift, because the top and bottom rows of the double-back shifter are shifted together at the same time.

FIG. 11 is useful for illustrating an example of a single column, single shift mode of operation for a continuous incoming stream of information units. In this example, a double-back shifter includes a top row of storage units **1101~1104** initially containing sequence indicators A~D and a bottom row of storage units **1105~1108** initially

containing sequence indicators E~H as shown in the figure. In order to perform a single shift operation instead of a double shift, at least one compare and reorder element or circuit in a third version of the reorder unit **200** employs the following first set of equations to provide equivalent results in this case as though compare and reorder, bottom row shift, and compare and reorder operations had been performed just prior to the shift.

$$A' = \max(A,E), \quad (1)$$

$$B' = \max(\max(B,F), \min(A,E)), \quad (2)$$

$$C' = \max(\max(C,G), \min(B,F)), \quad (3)$$

$$D' = \max(\max(D,H), \min(C,G)), \quad (4)$$

$$E' = \min(\min(A,E), \max(B,F)), \quad (5)$$

$$F' = \min(\min(B,F), \max(C,G)), \quad (6)$$

$$G' = \min(\min(C,G), \max(D,H)), \text{ and} \quad (7)$$

$$H' = \min(D,H), \quad (8)$$

where A'~D' are the reordered sequence indicators stored in the top row of storage units **1101~1104** just prior to the shift, and E'~H' are the reordered sequence indicators stored in the bottom row of storage units **1105~1108** just prior to the shift.

The first set of equations may then be modified as follows to form a second set of equations incorporating the final shift.

$$A'' = \max(\max(B,F), \min(A,E)), \quad (9)$$

$$B'' = \max(\max(C,G), \min(B,F)), \quad (10)$$

$$C'' = \max(\max(D,H), \min(C,G)), \quad (11)$$

D" = sequence indicator for

new information unit shifted in, (12)

$$E'' = \max(A,E), \quad (13)$$

$$F'' = \min(\min(A,E), \max(B,F)), \quad (14)$$

$$G'' = \min(\min(B,F), \max(C,G)), \quad (15)$$

$$H'' = \min(\min(C,G), \max(D,H)), \text{ and} \quad (16)$$

Sequence indicator for information unit shifted out of bottom row = $\min(D,H)$, (17)

where A"~D" are the reordered sequence indicators stored in the top row of storage units **1101~1104** just after the shift, and E"~H" are the reordered sequence indicators stored in the bottom row of storage units **1105~1108** just after the shift.

FIGS. 12A~12H illustrate, as a simplified example, the operation of a third version of the reorder cell unit **200**, employing a single column, single shift mode of operation for a limited stream of incoming information units. In **FIG. 12A**, the first row of a double-back shifter including storage units **1201~1208** is shown storing sequence indicators that are out of sequence. No compare and reorder operations are performed at this point, because the bottom row of the double-back shifter is assumed to contain invalid entries. In **FIG. 12B**, a single column shift of the top and bottom rows has occurred. In **FIG. 12C**, the first set of equations (1)~(8) above have been employed to compare and reorder the sequence indicators in the double-back shifter, resulting in the sequence indicators in storage units **1204** and **1205** getting reordered according to the following equations:

$$A = \max(A,E) = \max(3,1) = 3, \text{ and} \quad (18)$$

$$E = \min(\min(A,E), \max(B,F))$$

= min (min (3,1), max (invalid comparison))
= min (min (3,1) = 1. (19)

No other comparisons or changes were made in this simplified example, because the contents of storage units **1201** and **1206~1208** are assumed to be invalid entries. In **FIG. 12D**, a single column shift of the top and bottom rows has again occurred. In **FIG. 12E**, the first set of equations (1)~(8) above have again been employed to compare and reorder the sequence indicators in the double-back shifter, resulting in the sequence indicators in storage units **1204** and **1205** once again getting reordered according to the following equations:

A = max (A,E) = max (2,3) = 3, (20)
B = max (max (B,F), min (A,E))
= max (max (4,1), min (2,3))
= max (4, 2) = 4, (21)
E = min (min (A,E), max (B,F))
= min (min (2,3), max (4,1))
= min (2, 4) = 2), and (22)
F = min (min (B,F), max (C,G))
= min (min (4,1), max (invalid entry))
= min (min (4,1)) = 1. (23)

No other comparisons or changes were made in this simplified example, because the contents of storage units **1201~1202** and **1207~1208** are assumed to be invalid entries. In **FIG. 12F**, a single column shift of the top and bottom rows has again occurred. In **FIG. 12G**, the first set of equations (1)~(8) above have again been employed, but this time, resulting in no reordering of sequence indicators. Finally, in **FIG. 12H**, a single column shift of the top and bottom rows has again occurred, and the sequence indicators are shown to now be in proper sequence.

Although a fourth version of the reorder unit **200** may be implemented with a multi-column, single shift mode of operation, such a version will not be described herein, because its implementation is readily determinable from the prior discussions. All versions, however, are fully contemplated to be within the scope of the present invention.

FIG. 13 illustrates a block diagram of portions of a SONET network element including a plurality of sources including sources **101** and **1301** that transmit SONET payloads through a switch fabric including switch slices **105~109** to incoming buffers **104** of a destination **103'**. A staging shifter **300** is included in the destination **103'** to facilitate timely loading of information units from the incoming buffers **104** into the reorder unit **200**. The cell reorder unit **200** accommodates such a multiple source system by reordering information units only if they are from the same source. Also, although the prior examples described operations on a finite number or limited stream of information units and thus assumed many invalid information units for simplification purposes, in practice, the cell reorder unit **200** may handle a continuous stream of information units entering and leaving it, with only occasional and sporadic invalid information units being received. In particular, the number/frequency of invalid information units being received may be occasional or sporadic in a densely packed continuous stream of information units, or the number/frequency of invalid information units being received may be large in a sparsely packed and continuous stream of information units.

FIG. 14 illustrates, as an example, a block diagram including further detail on the relationship of the

incoming buffers **104**, the staging shifter **300** and the reorder unit **200**. The incoming buffers **104** include a plurality of path buffers, one for each path or switch slice in the SONET network element. Each path buffer receives incoming payloads from its assigned switch slice (e.g., path(1) buffer 1401 from switch slice(1) **105**, and path(K) buffer **1402** from switch slice(K) **109**). The staging shifter **300** includes a plurality of storage units, one for each path buffer. Each storage unit stores an information unit from its respective path buffer (e.g., information unit(1) stored in storage unit **301** from path(1) buffer **1401**, and information unit(K) stored in storage unit **302** from path(K) buffer **1402**). Information units for available SONET payloads or cells are preferably read in parallel periodically at the cell transfer rate from the path buffers into their respective storage units of the staging shifter **300**. The information units are then shifted serially into the reorder unit **200**, n-columns at a time upon each shift of the top row, wherein the integer "n" depends upon the mode of operation of the reorder unit **200**. The length of the double-back shifter is determined in this case by the number of paths in the SONET network element that may send information units to the destination, and the skew or difference of best case and worst case transit times for those information units through the switch slices. Also, since the maximum size of the sequence indicators is finite, the sequence indicators may wrap-around for long streams of SONET payloads. The compare and reorder logic in the cell reorder unit **200** detects such a wrap-around occurrence by, for example, inspection of the two most significant bits of the sequence indicator changing from "11" to "00".

FIG. 15 illustrates, as an example, a flow diagram of a method for reordering sequence indicated information

units into proper sequence for a limited stream or finite number of incoming information units. In **1501**, the method includes storing information units in a first shifter. As an example, this may involve receiving SONET payloads transmitted through a distributed switch fabric from one or more sources, and storing information units associated with the SONET payloads in the first shifter. For a finite stream, as in this example, the information units may be stored in parallel into the first shifter, whereas in a continuous stream, they would generally be shifted in one or more at a time. In **1502**, the method includes setting a counter N to integer 1. In **1503**, the method includes shifting the information units in the first shifter by one position, and storing a shifted out information unit in a second shifter. In **1504**, the method includes comparing information units stored in corresponding positions of the first and second shifters, and reordering the information units between the corresponding positions according to sequence information included in the information units. In a multiple source system, the reordering is only performed on information units between the corresponding positions if the information units are from a same source and valid. In **1505**, the method includes shifting the information units in the second shifter by one position. In **1506**, the method includes comparing information units stored in corresponding positions of the first and second shifters, and reordering the information units between the corresponding positions according to sequence information included in the information units. Again, in a multiple source system, the reordering is only performed on information units between the corresponding positions if the information units are from a same source and valid. In **1507**, the method includes checking the counter N to determine whether it has

incremented to a value K, which is generally equal to the number of columns in the top or bottom row of the double-back shifter. The minimum number of columns in this case is determined by the necessary number of iterations of **1503~1506** to shift the information units into and process through the second shifter so that they exit in proper sequence. If the method determines that the counter N has incremented to the value K, then the information units are ready to exit the second shifter in proper sequence. Therefore, in this case, in **1508**, the method includes shifting the information units out of the second shifter for further processing within the destination. For a finite stream, as in this example, the information units may be shifted out in parallel from the second shifter, whereas in a continuous stream, they would generally be shifted out one or more at a time. On the other hand, if the method determines that the counter N has not incremented to the value K, then in **1509**, it increments the counter N by 1, and jumps back to **1503** to continue repeating **1503~1509**, so as to shift the information units into and process through the second shifter so that they exit in proper sequence according to the sequence information included in the information units.

In a system employing a continuous stream of input and output information units, the counter N may be deleted. **FIG. 16** illustrates, as an example, a flow diagram of a method for reordering sequence indicated information units into proper sequence employing a single column, double shift mode of operation on a continuous stream of incoming information units. In **1601**, the bottom row of the double-back shifter is shifted. Shifting the bottom row first is preferable in this case, because it makes the first storage unit on the bottom row available for an information unit

that will be subsequently shifted into it when the top row is shifted, wherein the number of columns shifted depends upon the mode of operation of the double-back shifter. In **1602**, at least one circuit in the reorder unit **200** compares sequence indicators in corresponding sets of storage units in the double-back shifter, and reorders information units in associated storage units in the double-back shifter as necessary, wherein the corresponding sets of storage units and associated storage units depend upon the mode of operation of the double-back shifter. In **1603**, the top row of the double-back shifter is shifted, wherein the number of columns shifted depends upon the mode of operation of the double-back shifter. In **1604**, at least one circuit in the reorder unit **200** again compares sequence indicators in corresponding sets of storage units in the double-back shifter, and reorders information units in associated storage units in the double-back shifter as necessary. The method then repetitively performs **1601~1604** so that all information units are in proper sequence by the time they are shifted out of the double-back shifter.

FIG. 17 illustrates, as an example, a flow diagram of a method for reordering sequence indicated information units into proper sequence employing a single column, single shift mode of operation on a continuous stream of incoming information units. In this method, only a single shift is performed so that both top and bottom rows are shifted at the same time. **FIG. 18** illustrates, as an example, a flow diagram of a method for reordering sequence indicated information units into proper sequence employing a combined single column, single shift mode of operation on a continuous stream of incoming information units. The methods depicted in **FIGS. 17** and **18** are described in

reference to **FIGS. 11** and **12**, so they are not repeated here in order to avoid unnecessary redundancy.

Although the various aspects of the present invention have been described with respect to a preferred embodiment, it will be understood that the invention is entitled to full protection within the full scope of the appended claims.